

COURSE: Non CRS PATTERN

Name of the Faculty: Technology and Engineering

Name of the Programme: Master of Engineering- Electrical Engineering (Microprocessor System and Application)

Mode of Learning: REGULAR

Semester Number (For Example 01,02,03, etc.):					01								
Maximum Courses/Papers for the present Semester:					07								
Minimum Courses/Papers for the present Semester:					07								
Maximum marks for the present Semester:					550								
Minimum marks for the present Semester:					00								
Total Credits for the present Semester:					NIL								
Sr. No.	Department (NAME OF THE DEPARTMENT WHICH IS TEACHING THE PAPER)	Type of Course Core/ Elective/ Foundation/ IDE/ Compulsory etc.	Title of Paper	Group (if any)	Hours of Teaching per week [Credit*]	Teaching Learning Method [TLM]	Assessment Method [AM]	Assessment Type [AT] UA/IA	UA Marks	IA Marks	Total Marks	Minimum marks for Passing	Remarks for Minimum /Maximum Course/Paper/Subject/ Selection
1	Electrical Engineering	Core Compulsory	Advanced Microprocessor (ELE2137)	NA	04	Lecture	Theory	UA	70	--	100	40	UA=70 IA=30
								IA	--	30			
2	Electrical Engineering	Core Compulsory	Advanced Microprocessor (TW, Practical and Viva) (ELE2137L)	NA	03	Laboratory	Term Work, Practical and Viva	UA	50	--	50	20	UA=50
								IA	--	--			
3	Electrical Engineering	Core Compulsory	Microelectronics & VLSI Design (ELE2135)	NA	04	Lecture	Theory	UA	70	--	100	40	UA=70 IA=30
								IA	--	30			
4	Electrical Engineering	Core Compulsory	Microelectronics & VLSI Design (TW, Practical and Viva) (ELE2135L)	NA	03	Laboratory	Term Work, Practical and Viva	UA	50	--	50	20	UA=50
								IA	--	--			
5	Electrical Engineering	Core Compulsory	Applied Signal Processing & Filter Design (ELE2134)	NA	04	Lecture	Theory	UA	70	--	100	40	UA=70 IA=30
								IA	--	30			

6	Electrical Engineering	Core Compulsory	Applied Signal Processing & Filter Design (TW, Practical and Viva) (ELE2134L)	NA	03	Laboratory	Term Work, Practical and Viva	UA	50	--	50	20	UA=50
								IA	--	--			
7	Electrical Engineering	Core Compulsory	Communication Networks & Security (ELE2136)	NA	04	Lecture	Theory	UA	70	--	100	40	UA=70 IA=30
								IA	--	30			

Semester Number (For Example 01,02,03, etc.):					02								
Maximum Courses/Papers for the present Semester:					07								
Minimum Courses/Papers for the present Semester:					07								
Maximum marks for the present Semester:					550								
Minimum marks for the present Semester:					00								
Total Credits for the present Semester:					NIL								
Sr. No.	Department (NAME OF THE DEPARTMENT WHICH IS TEACHING THE PAPER)	Type of Course Core/ Elective/ Foundation/ IDE/ Compulsory etc.	Title of Paper	Group (if any)	Hours of Teaching per week [Credit*]	Teaching Learning Method [TLM]	Assessment Method [AM]	Assessment Type [AT] UA/ IA	UA Marks	IA Marks	Total Marks	Minimum marks for Passing	Remarks
1	Electrical Engineering	Core Compulsory	Artificial Intelligence & Machine Learning (ELE2236)	NA	04	Lecture	Theory	UA	70	--	100	40	UA=70 IA=30
								IA	--	30			
2	Electrical Engineering	Core Compulsory	Artificial Intelligence & Machine Learning (TW, Practical and Viva) (ELE2236L)	NA	03	Laboratory	Term Work, Practical and Viva	UA	50	--	50	20	UA=50
								IA	--	--			
3	Electrical Engineering	Core Compulsory	Image Processing & Computer Graphics (ELE2238)	NA	04	Lecture	Theory	UA	70	--	100	40	UA=70 IA=30
								IA	--	30			
4	Electrical Engineering	Core Compulsory	Image Processing & Computer Graphics (TW, Practical and Viva) (ELE2238L)	NA	03	Laboratory	Term Work, Practical and Viva	UA	50	--	50	20	UA=50
								IA	--	--			
5	Electrical Engineering	Core Compulsory	Embedded Applications in Industrial Control (ELE2235)	NA	04	Lecture	Theory	UA	70	--	100	40	UA=70 IA=30
								IA	--	30			

6	Electrical Engineering	Core Compulsory	Embedded Applications in Industrial Control (TW, Practical and Viva) (ELE2235L)	NA	03	Laboratory	Term Work, Practical and Viva	UA	50	--	50	20	UA=50
								IA	--	--			
7	Electrical Engineering	Core Compulsory	Computer Architecture & Parallel Processing (ELE2237)	NA	04	Lecture	Theory	UA	70	--	100	40	UA=70 IA=30
								IA	--	30			

Semester Number (For Example 01,02,03, etc.):					03 & 04									
Maximum Courses/Papers for the present Semester:					01									
Minimum Courses/Papers for the present Semester:					01									
Maximum marks for the present Semester:					300									
Minimum marks for the present Semester:					00									
Total Credits for the present Semester:					NIL									
Sr. No.	Department (NAME OF THE DEPARTMENT WHICH IS TEACHING THE PAPER)	Type of Course Core/ Elective/ Foundation/ IDE/ Compulsory etc.	Title of Paper	Group (if any)	Hours of Teaching per week [Credit*]	Teaching Learning Method [TLM]	Assessment Method [AM]	Assessment Type [AT] UA/ IA	UA Marks	IA Marks	Total Marks	Minimum marks for Passing	Remarks	
1	Electrical Engineering	Core Compulsory	ME Dissertation (ELE2404)	NA		Project	Dissertation	UA	300	--	300	120	UA=300	
								IA	--	--				

 सत्यं शिवं सुन्दरम्	FACULTY OF TECHNOLOGY AND ENGINEERING THE MAHARAJA SAYAJIRAO UNIVERSITY OF BARODA VADODARA Department of Electrical Engineering 2 year Post Graduate Course ME ELECTRICAL (Microprocessor System and Application)
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ME Electrical (Microprocessor System and Application) Part-I

	The Maharaja Sayajirao University of Baroda Faculty Technology and Engineering Department of Electrical Engineering		Academic Year	2021-22						
<u>ME Electrical (Microprocessor System and Application): Regular Programme</u>										
Year	I	ADVANCED MICROPROCESSOR	Credits / Hours per week				L: 4 hrs/week Pr. : 3hrs/week			
Semester	I	Year of Introduction: 2021 Year of Syllabus Revision: NIL	Maximum Marks / Grade				100+50			
Mode of Transaction			Lectures and Laboratory							
Course Outcome (CO) CO1 Make use of generic advanced microprocessor and internal organization and modes of operation of advanced microprocessors. CO2 Analyze addressing modes, instruction Sets and programing model of Advanced Microprocessors. CO3 Explain Processors application and basic architecture of Atom, Intel I3, I5, I7, AMD processors, MIPS processors and ARM Processors. CO4 Compile Advanced Programming with Handling Interrupts and Debugging.										
Unit No.	Topic/Unit		Contact Hours	Weightage (%)	BT Level	CO	PSO	Element s of Employability (Emp)/ Entrepreneurship (Ent)/ Skill Development (SD)	Relevance to Local (L)/National (N) Regional (R)/ Global (G)	Relation to Gender (G), Environment and Sustainability (ES), Human Values (HV) and Professional Ethics (PE)



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1	80486 And Family Microprocessors with Memory Management & Protection: Salient features, Internal architectures, Register organization, addressing modes, Signal descriptions, Real addressing mode, protected mode, virtual address mode, Privilege, Protection, Special operation, Bus interfaces, Basic Bus operation, Fetch cycles, Minimum system configurations, Interfacing memory and I/O devices with, Priority of bus use by 80x86, Bus Hold and HLDA sequence, Instruction set features, Coprocessor 80x87.	12	23	3,4	CO1 CO2	PSO1			
2	Pentium Microprocessor Family and Core2 Due: Introduction, real mode and protected mode operation, the software model of the Pentium, A functional description of the Pentium, Pentium processor registers, Pentium data organization, Pentium instruction types, Pentium addressing mode, Pentium instruction, MMX architecture.	08	15	3,4	CO1 CO2	PSO1			
3	Task and Task Switching: Introductory concepts, Task state segments, TSS descriptor, switching between tasks, Task gates, Task register, Nested tasks, Task scheduling, Extension of TSS length, I-O Bit map, changing privilege within a task changing LDTs.	06	12	3,4	CO1 CO2	PSO1			
4	Handling Interrupts and Debugging: Hardware and software exceptions, Exception processing. Interrupt descriptor table, Trap Gate, Interrupt gates, Task gate exception handlers and privilege levels, Error codes, Exception handler routines, Halt and shut down. Incompatibility, 80x86 debugging supports: Single stepping, Break point & Task switch break point, Segment selectors, loading segment selectors, Reading segment selector, attribute	07	13	3,4,6	CO1 CO2 CO4	PSO1 PSO3	SD	G	PE
5	Latest Processors: Overview of Architecture, Memory and organization of Atom, Intel I3, I5, I7, AMD processors, MIPS processors, SUN's Sparc processor, Mobile/Tablet processors	05	10	5	CO3	PSO1			



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6	ARM family of processors: Overview of ARM architecture, Modes of Operation, Instruction sets, Programming model, Android-ARM hardware- software interface	06	12	5	CO3	PSO1			
7	Advanced Programming: Floating point math, Interfacing to C: In line assembly, linking and full C to assembly templates, Fast calls.	08	15	3,4,6	CO1 CO2 CO4	PSO1 PSO3			
Reference Books									
1.	BARRY B. BREY, " THE INTEL MICROPROCESSORS-Architecture, Programming,and Interfacing", Pearson Education India. Eighth Edition								
2.	A. K. Ray & K. M. Bhurchandi- Advanced Microprocessor andPeripherals- Tata Mcgraw Hill.								
3.	The Pentium Microprocessor By Antonakos								
4.	Badri Ram , ‘Advanced Microprocessors and Interfacing’’, McGraw Hill, 2014								
5.	Steve Furber- ARM System-on-Chip Architecture								
6.	Intel® 64 and IA-32 Architectures Manual								
7.	Technical Resources: Intel® Core™ Processors								

Laboratory: 10-15 Experiments/Simulations based on Syllabus Contents.



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<u>ME Electrical (Microprocessor System and Application): Regular Programme</u>										
Year	I	Core / Elective / Foundation Applied Signal Processing and Filter Design	Credits / Hours per week				L: 4 hrs/week Pr. : 3hrs/week			
Semester	I	Year of Introduction: 2021 Year of Syllabus Revision: NIL	Maximum Marks / Grade				100+50			
Mode of Transaction		Lectures andLaboratory								
Course Outcome (CO) CO1: Illustrate applied aspects of various algorithms of transforming discrete time signal from time domain to frequency domain and vice versa CO2:Implement different type of discrete time systems/filters in view of their various characteristics. CO3: Design discrete time filters for various applications. CO4: Describe multirate signal processing, its implementation in terms of various filter banks, techniques of sampling rate conversion in time domain and frequency domain CO5: Apply concepts of multirate sampling and adaptive filtering for text, speech, audio and image transformation, coding and compression (3) CO6: Illustrate various power spectrum techniques.										
Unit No.	Topic		Contact Hours	Weightag (%)	BT Level	CO	PSO	Eleme nts of Employ ability (Emp)/ Entrepr eneursh ip(Ent)/ Skill Develo	Releva nce to Local (L)/ Nation al (N)/ Region al(R)/ Global (G)	Relatio n to Gender (G), Environment and Sustainabilit y (ES), Human Values (HV)and Professional



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							ment (SD)		Ethics (PE)
1	Discrete Fourier Transform: redundancy in DFT, The inverse transform, Circular convolution, Filtering of long data sequence, sectioned convolution, Twiddle factor, Fast Fourier transform FFT Algorithms for convolution & correlations	09	17	3,4	CO1 CO2	PSO1 PSO3 PSO4	SD	G	PE
2	Structures for Discrete Time Systems; Structures of filters : Direct Form 1 & 2, Parallel, Cascade, Canonic realizations, Lattice structures; Fixed-Point & Binary Floating-point Representation of numbers, Errors Resulting from Rounding and Truncation, Analysis of Finite wordlength effects, Quantization effects on Filter Coefficients in FIR Filters, Round-Off Effects in Digital Filters	07	08	3,4	CO1 CO2	PSO1 PSO3 PSO4			
3	Filter Design Procedures: Design of IIR& FIR filters. IIR design techniques; via analog conversion, Butterworth, Chebyshev, Bessel's filters. A generalized design procedure for IIR filters. FIR designs via Ideal low pass filters, Time domain window functions. Low pass FIR filter design procedure.	11	25	3,4,5	CO1 CO2 CO3	PSO1 PSO3 PSO4 PSO5			
4	Multirate digital signal processing: interpolator, Decimator, multistage implementation of sampling rate conversion, sampling rate conversion by an arbitrary factor	06	08	4	CO4	PSO1 PSO3 PSO4			
5	Applications of multi rate signal processing, multirate	10	24	4,3	CO4	PSO1			



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	filter banks and subband coding, digital speech coding, speech signal analysis and Transform coding, Hilbert Transform, Haar transform, Wavelet transform; Adaptive filtering, Minimum mean square criterion, Wiener filter, LMS adaptive algorithm				CO5	PSO3 PSO4 PSO5			
6	Power spectrum estimation, Estimation of Spectra from Finite-duration Observations of signals Estimation of the Autocorrelation and Power spectrum estimation of Random Signals, The Periodogram, Use of DFT in power spectrum estimation. Parametric methods of power spectrum estimation, Eigen analysis Algorithms for Spectrum estimation- MUSIC, ESPRIT algorithm	09	18	3	CO6	PSO1 PSO3 PSO4 PSO5			
Reference Books									
1.	Digital Signal Processing: Principles, Algorithms and Applications: John G. Proakis and Dimitris G. Manolakis (Prentice Hall India)								
2.	Digital Signal Processing: A Computer Based approach: Sanjit K. Mitra (Tata McGraw Hill)								
3	Digital Signal Processing – A practical Approach: Emmanuel Ifeachor and Barry Jervis, Addison Wesley publishing company								
4	Digital Signal Processing Using MATLAB & Wavelets, Michael Weeks, 2 nd edition, INFINITY SCIENCE PRESS								
5.	Discrete-Time Signal Processing: A.V. Oppenheim and R.S. Schaffer (Prentice Hall India)								
6	Digital Signal Processing Using MATLAB Vinay K. Ingle, John G. Proakis, 3rd Edition, 2012, Cengage learning								

Laboratory : 6-12 Experiments/Simulations based on Syllabus Contents.

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	The Maharaja Sayajirao University of Baroda Faculty Technology and Engineering Department of Electrical Engineering					Academic Year		2021-2022				
Year	I	Core / Elective / Foundation Communication Networks and Security				Credits / Hours per week		4 hrs/week				
Semester	I	Year of Introduction: 2021 Year of Syllabus Revision:NIL				Maximum Marks / Grade		100				
Mode of Transaction		Lectures										
COURSE OUTCOMES:												
• CO1 Demonstrate the understanding of concepts of Data Communication and networks, layered architecture and their applications. • CO2 Analyse different Layers protocols. • CO3 Evaluate data communication link considering elementary concepts of data link layer protocols for error detection and correction. • CO4 Evaluate different network security techniques. • CO5 Explain basic concept of Wireless sensor network. • CO6 Explain architecture and different applications of IoT.												
Unit No.	Topic				Contact Hours	Weightage (%)	BT Level	CO	PSO	Elements of Employability (Emp)/ Entrepreneurship	Relevance to Local (L)/ National (N)/ Regional	Relation to Gender (G), Environment and Sustainability (ES), Human Values (HV)



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							(Ent)/ Skill Develop ment (SD)	al (R)/ Glob al (G)	and Professional Ethics (PE)
1	Overview of Communication Methods: Serial and parallel communication, Asynchronous and synchronous transmission, Circuit and packet switching, network architecture and the OSI model.	6	12	2,4	CO1 CO2	PSO1 PSO3 PSO5	SD	G	PE
2	Medium Access and Data link Layer: (12) Polling, token passing and random access, LANs IEEE 802.n procedures, ALOHA protocols, CSMA, Demand assignment, Packet radio, Data-link layer design issues, error handling and flow control, CRC, checksum, ARQ, sliding window protocols, HDLC, SDLC, BSC, XMODEM protocols	12	24	2,4,5	CO1 CO2 CO3	PSO1 PSO3 PSO5			
3	Network Layer: IP addressing, routing algorithms, Congestion control and Resource allocation, Quality of Service 12)	12	22	2,4,5	CO1 CO2 CO3	PSO1 PSO3 PSO5			
4	Network Security: Security attacks, cryptography building blocks, RSA, Authentication protocols, IP security, Transport layer security, wireless security, pretty good privacy (PGP), Firewall. (05)	6	12	2,5	CO1 CO4	PSO1 PSO3 PSO5			



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5	Wireless Embedded Networking: Wireless sensor networks – Introduction, Applications, Network Topology, Localization, Time Synchronization, Energy efficient MAC protocols, SMAC, Energy efficient and robust routing , Data Centric routing.	8	15	4,5	CO2 CO5	PSO1 PSO3 PSO5			
6	IoT Architecture: History of IoT, M2M (Machine to Machine), Web of Things, IoT protocols, Remote monitoring and sensing, remote controlling, Performance analysis, IoT Protocol architecture and communication pattern.	8	15	2,4,5	CO1 CO2 CO6	PSO1 PSO3 PSO5			
References :									
1.	Computer Networks; By: Tanenbaum, Andrew S; Pearson Education Pte. Ltd., Delhi, 4th Edition								
2.	Computer Networks: A Systems Approach by Larry Peterson and Bruce Davie, fifth edition.								
3.	Data and Computer Communications; By: Stallings, William; Pearson Education Pte. Ltd., Delhi, 8th Edition								
4.	6LoWPAN: The Wireless Embedded Internet, Zach Shelby, Carsten Bormann, Wiley								
5.	Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. Ovidiu Vermesan, Dr. Peter Friess, River Publishers								
6.	Holger Karl and Andreas Wiilig, “Protocols and Architectures for Wireless Sensor Networks” John Wiley & Sons Limited 2008.								

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<u>ME Electrical (Microprocessor System and Application): Regular Programme</u>												
Year	I	Core / Elective / Foundation MICROELECTRONICS AND VLSI DESIGN				Credits / Hours per week			L: 4 hrs/week Pr. : 3hrs/week			
Semester/ Part	I	Year of Introduction: 2021 Year of Syllabus Revision: NIL				Maximum Marks / Grade			100+50			
Mode of Transaction		Lectures and Laboratory										
Course Outcome (CO)												
CO1 <u>Comprehend</u> the various VLSI design styles, approaches												
CO2 <u>Analyze</u> MOS based VLSI circuits working under linear and saturation region of operation.												
CO3 <u>Explain</u> the process of developing standard cell library and its characterization process.												
CO4 <u>Make use of</u> HDL-VHDL & Verilog, Detail study of HDL Tool for synthesis and simulation, FPGA & CPLD programming.												
CO5 <u>Develop</u> Digital System Design using VHDL with different Models for design in details.												
CO6 <u>Develop</u> Design libraries & attributes. CPU modeling & design.												
Unit No.	Topic/Unit				Contact Hours	Weightage (%)	BT Level	CO	PSO	Elements of Employability (Emp)/ Entrepreneurship (Ent)/ Skill Development (SD)	Relevance to Local (L)/ National (N)/ Regional (R)/ Global (G)	Relation to Gender (G), Environment and Sustainability (ES), Human Values (HV)and



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									Professional Ethics (PE)
1	Introduction to VLSI: Introduction, Design methodology, Level of abstractions, Design flow, Design approaches, Design styles, Design considerations, Design quality-reliability- updateability, EDA tools	08	15	2	CO1	PSO2 PSO3	SD	G	PE
2	MOS Transistor: The MOS structure, The MOS under external Bias, Structure and Operation of MOS Transistor, Current-Voltage Characteristic, Scaling and Small Geometry Effects, MOS Inverter: Generalized MOS inverter, MOS inverter with various loads, CMOS inverter, Definition and Calculation of Delay, Delay-Power product,	12	25	4	CO2	PSO2 PSO3			
3	Standard Cell Library Design and Characterization: Schematic and Layout Design, Extraction from layout, Standard cell library data, Cell Characterization, Power Characterization, Reliability and Noise Characterization, Interconnect delay modeling.	06	10	5	CO3	PSO2 PSO3			
4	Computer Aided Digital System Design: HDL, HDL capabilities, Design Synthesis, Design Tool Flow, H/W simulation, Computer based design process tools, Designing with VHDL: Basic concepts in VHDL, Architecture, Timing and concurrency, objects and classes, Conventions and syntax problems, Structural specification of hardware, parts library.	10	20	3	CO4	PSO2 PSO3			
5	Behavioral Description of H/W: Process statements, assertion statements, sequential statements, wait statements, Dataflow description in VHDL: State machine description, Dataflow circuit, Structural modeling.	10	20	6	CO5	PSO2 PSO3			
6	Advance Features: Subprograms & packages, Predefine Attributes, Generics & Configurations, Generate Statements, CPU Modeling and Design, Modeling a test bench, Introduction to Verilog.	06	10	3	CO6	PSO2 PSO3			
Reference Books									



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1.	ZaiclabinNavabi., “VHDL- Analysis and Modeling of Digital System”, McGraw Hill
2.	Dauglas Perry., “VHDL”, Prentice Hall of India
3.	Kevin Skahil ., “VHDL”, Addison Wesley
4.	JayramBhasker., “A VHDL Primer”, PHI
5.	Neil & Kamran., “Principal of CMOS VLSI Design”, Addison Wesley
6.	Douglas A Pucknell& Kamran Eshraghian., “Basic VLSI Design”, PHI
7.	Kang and Leblebici., “CMOS Digital Integrated Circuits”, Tata McGraw Hill
8.	Debaprasad Das., “VLSI Design”, Oxford University Press

Laboratory : 10-12 Experiments/Simulations based on Syllabus contents.

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<u>ME Electrical (Microprocessor System and Application): Regular Programme</u>										
Year	I	Core / Elective / Foundation Artificial Intelligence and Machine Learning	Credits / Hours per week				L: 4 hrs/week Pr. : 3hrs/week			
Semester	II	Year of Introduction: 2021 Year of Syllabus Revision: NIL	Maximum Marks / Grade				100+50			
Mode of Transaction		Lectures and Laboratory								
Course Outcome (CO) CO1: Explain working and applications of various Artificial Neural Network CO2: Describe various types of estimators based on Regression analysis CO3: Apply various adaptive filtering algorithms for estimation and prediction CO4: Apply Kernel methods in view of Radial Bases function Networks CO5: Apply support vector machine principles to find optimal solutions CO6: Apply Multi-objective optimization algorithms										
Unit No.	Topic		Contact Hours	Weightage (%)	BT Level	CO	PSO	Elements of Employability (Emp)/ Entrepreneurship (Ent)/ Skill Development (SD)	Relevance to Local (L)/ National (N)/ Regional (R)/ Global (G)	Relation to Gender (G), Environment and Sustainability (ES), Human Values (HV) and Professional Ethics (PE)



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1	Artificial Neural Network: Model of Neuron, NN viewed as Directed Graphs, Network Architecture, Learning Process, Learning Task, Perceptron, Convergence theorem, relation between the perceptron and Bayes Classifier, Pattern Classifier, Batch perceptron algorithm, Multi level perceptron: Batch Learning and On-Line Learning, The Back-Propagation Algorithm, Pattern Classification The Hessian and Its Role in On-Line Learning, Optimal Annealing and Adaptive Control of the Learning Rate, Supervised Learning Viewed as an Optimization Problem, Convolutional Networks, Nonlinear Filtering	10	22	2,3,4	CO1	PSO3 PSO4 PSO5	SD	G	PE
2	Model Building through regression: Linear regression model, Maximum a Posteriori Estimation of the Parameter Vector, Relationship Between Regularized Least-Squares Estimation and MAP Estimation, Pattern Classification, The Minimum-Description-Length Principle, Finite Sample-Size Considerations, The Instrumental-Variables Method	08	12	2,3,4	CO2	PSO3 PSO4 PSO5			
3	Filtering Structure of the LMS Algorithm, Unconstrained Optimization, The Wiener Filter, The Least-Mean-Square Algorithm, Markov Model Portraying the Deviation of the LMS Algorithm from the Wiener Filter, The Langevin Equation: Characterization of Brownian Motion,	09	16	2,3,4	CO3	PSO3 PSO4 PSO5			



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	Kushner's Direct-Averaging Method, Statistical LMS Learning Theory for Small Learning-Rate Parameter, Linear Prediction, Pattern Classification								
4	Kernel methods and Radial Bases function Networks: Cover's Theorem on the Separability of Patterns Radial-Basis-Function Networks, K-Means Clustering, Recursive Least-Squares Estimation of the Weight Vector, Pattern Classification, Principles of Self-Organization, Self organizing Maps. Principal-Components Analysis: Perturbation Theory, Hebbian-Based Principal-Components Analysis, Kernel Principal-Components Analysis, Kernel Hebbian Algorithm	09	15	2,3,4	CO4	PSO3 PSO4 PSO5			
5	Support Vector machine: Optimal Hyperplane for Linearly Separable Patterns, Optimal Hyperplane for Nonseparable Patterns, The Support Vector Machine Viewed as a Kernel Machine, Design of Support Vector Machines, Pattern Classification, Optimal Solution of the Linear Regression Problem	07	15	2,3,4	CO5	PSO3 PSO4 PSO5			
6	Multi-objective optimization using Evolutionary algorithm: Classical Multi-objective optimization problem, Multi-objective Genetic Algorithm, Evolution strategies, Evolutionary programming, Genetic programming, Multi-modal function Optimization	09	20	2,3,4	CO6	PSO3 PSO4 PSO5			



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Reference Books

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|----|---|
| 1. | Neural network and Learning Machines- Simon Haykin – 3 rd Edition Pearson – Prentice hall - |
| 2. | Multi-objective optimization using Evolutionary algorithm- Kalyanmoy Deb- Wiley Interscience series in systems and optimization, 2001 |

Laboratory : 10-12 Simulations/Experiments based on Syllabus contents.

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 सत्यं शिवं सुन्दरम्		The Maharaja Sayajirao University of Baroda Faculty of Technology and Engineering Department of Electrical Engineering		Academic Year				2021-22			
ME Electrical (Microprocessor System and Application): Regular Programme											
Year	I	Core / Elective / Foundation Computer Architecture & Parallel Processing		Credits / Hours per week				L: 4 hrs/week			
Semester / Part	II	Year of Introduction: 2021 Year of Syllabus Revision: NIL		Maximum Marks / Grade				100			
Mode of Transaction		Lectures									
Course Outcome (CO) CO1: <u>Examine</u> the applicability and implementation of single cycle (MIPS), multi-cycle (MIPS) and pipelined architectures. CO2: <u>Analyze</u> the performance and design trade-offs in designing and constructing a computer processor including memory. CO3: <u>Assess</u> the limitations of classical architectures and the importance of parallelism CO4: <u>Illustrate</u> the elements of modern instructions sets and their impact on processor design. CO5: <u>Compare</u> the characteristics of shared memory and distributed multiprocessor systems and cache coherency protocols. CO6: <u>Analyze</u> the principles in instruction set design including Superscalar and RISC architectures.											
Unit No.	Topic			Contact Hours	Weightage (%)	BT Level	CO	PSO	Elements of Employability (Emp)/ Entrepreneurship (Ent)/ Skill Development	Relevance to Local (L)/ National (N)/ Regional (R)/ Global (G)	Relation to Gender (G), Environment and Sustainability (ES), Human Values (HV) and Professional Ethics (PE)



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							ment (SD)	bal (G)	
1	Introduction to Parallel Processing: Memory and input-output subsystems - hierarchical memory structure, virtual memory system, memory allocation and management, input-output subsystem, Cache memories and management. Principles of Pipelining and vector processing: Pipelining - an overlapped parallelism - instruction and arithmetic pipeline - principles of designing pipeline processors, vector processing requirements.	12	25	4,4,5, 4	CO1 CO2 CO3 CO5	PSO1 PSO4	SD	G	PE
2	Instruction set principles – Classifying instruction set architecture, the MIPS architecture, memory addressing, Operations in the instruction sets, instruction for control flow, Datapath and control implementation for single cycle, Multi-cycle and Pipelined processors. Techniques to handle hazards, performance improvement with pipelines and effect of hazards on the performance.	10	20	4,4	CO1 CO4	PSO1 PSO4			
3	Thread Level Parallelism - Introduction, Shared-Memory Multicore Systems, Performance Metrics for Shared-Memory Multicore Systems, Cache Coherence Protocols, Synchronization, Memory Consistency, system deadlock and protection, Inter-connection networks, exploiting concurrence for multiprocessing.	08	15	4	CO5	PSO1 PSO4			



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4	Data Level Parallelism Introduction, Vector Architecture, Enhancing Vector Performance & Performance evaluation. SIMD Instruction Set Extensions for Multimedia, Graphics Processing Units, GPU Memory Hierarchy, Detecting and Enhancing Loop- Level Parallelism	08	15	5,4	CO3 CO4	PSO1 PSO4			
5	Reduced Instruction Set Components (RISC): Instruction Execution characteristics, Use of a large register file, Compiler based register optimizations, RISC architecture, Introduction to RISC-V.	08	14	4,4	CO2 CO6	PSO1 PSO4			
6	Superscalar and VLIW Architecture - CPU structure and function. Super Harvard Architecture. Plug & Play / USB Architecture.	06	11	4,4	CO2, CO6	PSO1 PSO4			
Reference Books									
1.	Computer Organization & Architecture (PHI)-By William Stallings								
2.	Computer Architecture: A quantitative approach- By John Hennessey & David Patterson								
3.	Structured Computer Organization by Tannenbaum								
4.	Computer System Architecture (PHI) By M.Morris Mano								
5.	Computer Organization & Design: The hardware/software interface – By John Hennessey & David Patterson								
6.	Parallel Computer Architecture: A Hardware / Software Approach - David Culler, Jaswinder Pal Singh&Anoop Gupta								

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<u>ME Electrical (Microprocessor System and Application): Regular Programme</u>				
Year	I	Core / Elective / Foundation Embedded Applications in Industrial Control	Credits / Hours per week	L: 4 hrs/week Pr. : 3hrs/week
Semester	II	Year of Introduction: 2021 Year of Syllabus Revision: NIL	Maximum Marks / Grade	100+50
Mode of Transaction		Lectures and Laboratory		
Course Outcome (CO)				
CO1: Design embedded system for industrial applications by interfacing different components of the system. CO2:Develop embedded programs for low power microcontrollers for robotic applications. CO3: Create ARM based basic and advanced programs for MEMs sensor-based applications. CO4: Assess the different type of sensors, signal conditioning elements and Controller principles for real life applications. CO5:Develop PLC Ladder diagram for variousreal-world problems/applications. CO6:Explain the architecture and features of a digital signal processor for real-time implementations.				



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Unit No.	Topic	Contact Hours	Weightage (%)	BT Level	CO	PSO	Element s of Employ ability (Emp)/ Entrepre neurship (Ent)/ Skill Develop ment (SD)	Releva nce to Local (L)/ Nationa l (N)/ Region al(R)/G lobal (G)	Relation to Gender (G), Environ ment and Sustaina bility (ES), Human Values (HV)and Professio nal Ethics (PE)
1	Introduction to embedded systems, Classification of architecture models, Networking in Embedded systems-(I2C, CANBUS, MODBUS, USB), Serial and Parallel port interfaces, High-speed I/O interfacing, Transducers and their interfacing.	10	16	5,6	CO1 CO4	PSO1	Ent	G	PE
2	Microcontrollers based Industrial Applications: Development of PID control Algorithm in Assy Lang. and controlling temperature through ON/OFF control or proportionate control. Interfacing of keyboard & 7-Segment Led Display & Lcd display, Industrial timer/counter, Power factor & Frequency measurement, Waveform generation using DAC, stepper motor	16	35	6	CO1 CO2	PSO1 PSO3			



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	controller. Interfacing of I2C EEprom&Dac. Interfacing of Serial Printer using UART/RS232, HMI interfacing through RS485-Modbus communication protocol.								
3	Controlling Principles and Methods, Design of analog/digital controllers, Discrete State Process Control, PLC Architecture and ladder logic programming, Industrial applications using PLC.	10	20	5,6	CO4 CO5	PSO1 PSO3			
4	C8051F340 microcontroller & Applications: Introduction to C8051F340 microcontroller, advance features e.g. ADC, USB, etc. Interfacing DC BLDC motor using PWM & interfacing IR sensors for Line follower robot. Open loop Speed control of DC motor.	06	10	6	CO1 CO2	PSO1 PSO3			
5	DSP Overview: Architecture, Computing Unit IEEE floating point operation, multifunction computing, address generation, program sequencer, instruction cycle & operation, Interrupts, Timer, memory buses & interfacing, internal data transfer & context switching, hardware design, software preliminaries, syntax code notation, tools, Applications for servo control.	06	14	5	CO6	PSO1 PSO4			
6	Introduction to Cortex M7 microcontroller STM32F746: Enhanced Features, Block Diagram & Basic functions. Interfacing with MEM sensors, Accelerometer, Gyro.	04	05	6	CO3	PSO1 PSO3			
Reference Books									



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1.	Interfacing Sensors to the IBM PC – W. Tompkins, J.G. Webster (PH Intl)
2.	Process Control Instrumentation Technology - Curtis D Johnson (4rth Ed.)
3.	D.V. Hall : Microprocessors And Interfacing, Programming and hardware.
4.	Datasheets for C8051F340 and Cortex-M7.
5.	Manuals for DSP Processor (C28X)

Laboratory : 10-15 Experiments/Simulations based on Syllabus Contents.

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<u>ME Electrical (Microprocessor System and Application): Regular Programme</u>			
Year	I	Core / Elective / Foundation Image Processing and Computer Graphics	Credits / Hours per week L: 4 hrs/week Pr. : 3hrs/week
Semester / Part	II	Year of Introduction: 2021 Year of Syllabus Revision: NIL	Maximum Marks / Grade 100+50
Mode of Transaction	Lectures and Laboratory		
Course Outcome (CO) CO1: Demonstrate the understanding of fundamental concepts of a digital image processing system. CO2: Evaluate the techniques for image enhancement, image restoration, image segmentation and spatial filtering. CO3: Formulate techniques of image compression and analysis images using morphology tools and transforms technique to modify the images. CO4: Have a knowledge and understanding of the structure of an interactive computer graphics system. CO5: Analyze the various algorithm for drawing basic shapes in geometry and to scan, convert the basic geometrical primitives, transformations, Area filling, clipping.			



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Unit No.	Topic	Contact Hours	Weightage (%)	BT Level	CO	PSO	Element s of Employa bility (Emp)/ Entrepre neurship (Ent)/ Skill Develop ment (SD)	Relevan ce to Local(L)/ National (N)/ Regional (R)/Glob al (G)	Relatio n to Gender (G), Enviro nment and Sustain ability (ES), Human Values (HV)an d Profess ional Ethics (PE)
1.	DIGITAL IMAGE FUNDAMENTALS AND INTENSITY TRANSFORMATION: Light, Brightness adaption and discrimination, Pixels, sampling and quantization., Basic gray level Transformations, Histogram Processing, Histogram equalization, Histogram Matching, Histogram for Image Enhancements, Color Fundamentals, Color Models,	06	10	2,5	CO1 CO2	PSO3 PSO4	SD	G	PE
2.	FILTERING IN THE SPATIAL DOMAIN AND FREQUENCY DOMAIN:	06	15	5	CO2	PSO3 PSO4			



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	Correlation and convolution, Smoothing filters, sharpening filters, gradient and Laplacian., Frequency domain filtering. , Discrete Cosine Transform, Fourier Transform, Wavelet Transform								
3.	IMAGE RESTORATION, RECONSTRUCTION AND COMPRESSION Image Restoration techniques, Noise characterization, Noise restoration filters, Adaptive filters, Types of redundancies, Lossy and Lossless compression, Huffman Coding, Arithmetic Coding, , LZW coding, Transform Coding, DCT implementation using FFT, Run length coding, JPEG, Lossless predictive coding, Lossy predictive coding	08	15	5,5	CO2 CO3	PSO3 PSO4			
4.	IMAGE SEGMENTATION AND MORPHOLOGICAL OPERATIONS: Boundary detection based techniques, Point, line detection, Edge detection, Edge linking, local processing, regional processing, Hough transform, Thresholding, Otsu's method, Region-based segmentation, Watershed algorithm, Use of motion in segmentation. Erosion, Dilation, Opening, Closing, Hit-or-Miss Transform, Boundary Detection, Hole filling, connected components, convex hull, thinning, thickening, skeletons, pruning, Geodesic Dilation, Erosion, Reconstruction by dilation and erosion.	10	20	5	C03	PSO3 PSO4			
5.	INTERACTIVE GRAPHICS: Uses of Computer Graphics; Classification of applications. Development	06	10	2	C04	PSO4			



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	of Hardware & Software for computer graphics, conceptual framework for interactive graphics. Graphics System: Video Display Devices, Refresh C.R.Ts, Raster Scan & Random Scan Displays D.V.S. T., Color C.R.T. & Input devices, Graphic Standards.								
6.	GRAPHIC PRIMITIVES : Algorithms for Line Drawing, (DDA Bresenham's) Bresenham's general algorithm for line drawing, Cohen sutherland line clipping algorithm, Bresenham's Circle ,Ellipse & other curves drawing algorithm, Midpoint circle algorithm. Filled Area, Scan line polygon area, Boundary fill & flood fill (Edge fill, Fence fill, Seed fill), Inside/Outside test, Midpoint line drawing algorithm	16	30	5	C05	PSO3 PSO4			
Reference Books									
1.	Procedural Elements Of Computer Graphics By David F.Rogers, Publisher : McGraw Hill, Second Edition								
2.	Computer Graphics by Donald Hearn & M Pauline Baker, Second Edition, Publisher: Prentice Hall, 2000								
3.	Gonzalez Rafael C and Woods Richard E, Digital Image Processing, 3rd Edition, Prentice Hall, 2008.								
4.	Pitas Ioannis, Digital Image Processing Algorithms and Applications, John Wiley, 2000.								
5.	Jain Anil K, Fundamentals of Digital Image Processing, Prentice Hall, 1989								

Laboratory : 10-15 Experiments/Simulations based on Syllabus Contents.